CLAIMS:

1. A method of forming a thin film transistor over a substrate comprising the following steps:

providing a layer of semiconductive material from which a channel region and at least one of a source region or a drain region of a thin film transistor are to be formed; and

conductively doping the at least one of the source region or the drain region of the semiconductive material layer while preventing conductivity doping of the channel region of the semiconductive material layer, such doping being conducted without any masking of the channel region by any separate masking layer.

2. The method of forming a thin film transistor of claim 1 wherein the one of the source region or the drain region is elongated and the channel region is elongated, the channel region being oriented substantially perpendicularly relative to the one region.

3. The method of forming a thin film transistor of claim 1 wherein the one region is elongated and oriented substantially parallel with the substrate, and the channel region is elongated and oriented substantially perpendicularly relative to the substrate and one region.

4. The method of forming a thin film transistor of claim 1 comprising doping the source region and the drain region in a single step.

5. A method of forming a thin film transistor over a substrate comprising the following steps:

providing a layer of semiconductive material from which a source region, a drain region and a channel region of a thin film transistor are to be formed; and

conductively doping the source region and the drain region of the semiconductive material layer while preventing conductivity doping of the channel region of the semiconductive material layer, such source region doping and such drain region doping being conducted without any masking of the channel region by any separate masking layer.

6. The method of forming a thin film transistor of claim 5 wherein the source region and the drain region are oriented parallel relative to one another, the channel region being oriented substantially perpendicularly relative to the source and drain regions.

7. The method of forming a thin film transistor of claim 5 wherein the source region and the drain region are oriented substantially parallel with one another and the substrate, the channel region being oriented substantially perpendicularly relative to the substrate and the source and drain regions.

8. The method of forming a thin film transistor of claim 5 comprising doping the source region and the drain region in a single step.

9. A method of forming a thin film transistor comprising the following steps:

providing a substrate having a node to which electrical connection is to be made;

providing a first electrically insulative dielectric layer over the substrate;

providing an electrically conductive gate layer over the first dielectric layer;

providing a second electrically insulative dielectric layer over the electrically conductive gate layer;

providing a contact opening through the second dielectric layer, the electrically conductive gate layer and the first dielectric layer; the contact opening defining projecting sidewalls;

providing a gate dielectric layer within the contact opening laterally inward of the contact opening sidewalls;

providing a layer of semiconductive material over the second dielectric layer and within the contact opening against the gate dielectric layer and in electrical communication with the node; the semiconductive material within the contact opening defining an elongated and outwardly extending channel region the electrical conductance of which can be modulated by means of the adjacent electrically conductive gate and gate dielectric layers; and

conductively doping the semiconductive material layer lying outwardly of the contact opening to form one of a source region or a drain region of a thin film transistor.

10. The method of forming a thin film transistor of claim 9 wherein the step of providing the semiconductive material layer comprises only partially filling the contact opening to define an annulus within the contact opening, the channel region comprising the annulus.

11. The method of forming a thin film transistor of claim 9 wherein the projecting sidewalls are provided to be substantially perpendicular relative to the substrate.

12. The method of forming a thin film transistor of claim 9 wherein the step of providing the semiconductive material layer comprises only partially filling the contact opening to define an annulus within the contact opening, the channel region comprising the annulus, and wherein the projecting sidewalls are provided to be substantially perpendicular relative to the substrate.

13. The method of forming a thin film transistor of claim 9 wherein the step of providing the gate dielectric layer comprises:

depositing a gate dielectric layer over the second dielectric layer and to within the contact opening, the deposited gate dielectric layer less than completely filling the contact opening; and

anisotropically etching the gate dielectric layer to define a gate dielectric layer annulus within the contact opening.

14. The method of forming a thin film transistor of claim 9 wherein the layer of semiconductive material is provided to completely fill the contact opening.

15. The method of forming a thin film transistor of claim 9 wherein the step of providing the gate dielectric layer comprises:

depositing a gate dielectric layer over the second dielectric layer and to within the contact opening, the deposited gate dielectric layer less than completely filling the contact opening; and

anisotropically etching the gate dielectric layer to define a gate dielectric layer annulus within the contact opening; and

wherein the step of providing the semiconductive material layer comprises only partially filling the contact opening to define the channel region is the shape of an annulus within the contact opening.

16. The method of forming a thin film transistor of claim 9 wherein the step of providing the gate dielectric layer comprises:

depositing a gate dielectric layer over the second dielectric layer and to within the contact opening, the deposited gate dielectric layer less than completely filling the contact opening; and

anisotropically etching the gate dielectric layer to define a gate dielectric layer annulus within the contact opening;

wherein the step of providing the semiconductive material layer comprises only partially filling the contact opening to define the channel region is the shape of an annulus within the contact opening; and

wherein the projecting sidewalls are provided to be substantially perpendicular relative to the substrate.

17. The method of forming a thin film transistor of claim 9 wherein the one region is provided run substantially parallel with the substrate.

18. The method of forming a thin film transistor of claim 9 wherein,

the step of providing the contact opening comprises:

providing an initial contact opening through the second electrically conductive layer to the electrically conductive gate layer;

providing a preliminary electrically insulative layer over the second dielectric layer and to within the initial contact opening, the deposited preliminary electrically insulative layer less than completely filling the initial contact opening; and

anisotropically etching the primary electrically insulative layer to define an insulative spacer within the initial contact opening; and

the step of providing the gate dielectric layer comprises:

providing a secondary contact through the gate layer and the first dielectric layer using the insulative spacer as an etching mask;

providing a secondary electrically insulative layer over the second dielectric layer, the insulative spacer and to within the secondary contact opening, the deposited secondary electrically insulative layer less than completely filling the secondary contact opening; and

anisotropically etching the secondary electrically insulative layer to define a gate dielectric layer annulus within the secondary contact opening.

19. A product produced by the process of claim 18.

20. A thin film transistor comprising:

a thin film transistor layer having a source region, a channel region and a drain region; and

a gate in proximity to the thin film channel region, the gate comprising an annulus which encircles the thin film channel region.

21. The thin film transistor of claim 20 wherein the gate annulus is longitudinally elongated.

22. The thin film transistor of claim 20 wherein at least one of the source region or the drain region is elongated and the channel region is elongated, the channel region being oriented substantially perpendicularly relative to the one region.

23. The thin film transistor of claim 20 wherein the source region and the drain region are elongated and oriented parallel relative to one another, the channel region being elongated and oriented substantially perpendicularly relative to the source and drain regions.

24. The thin film transistor of claim 20 wherein the thin film transistor is provided relative to a supporting substrate, the gate annulus being longitudinally elongated and oriented substantially perpendicularly relative to the substrate.

25. A thin film transistor comprising:

a thin film transistor layer having a source region, a channel region and a drain region; the thin film channel region comprising an annulus; and

a gate in proximity to the thin film channel annulus.

26. The thin film transistor of claim 25 wherein the channel annulus is longitudinally elongated.

27. The thin film transistor of claim 25 wherein at least one of the source region or the drain region is elongated and the channel region is elongated, the channel region being oriented substantially perpendicularly relative to the one region.

28. The thin film transistor of claim 25 wherein the source region and the drain region are oriented parallel relative to one another, the channel region being oriented substantially perpendicularly relative to the source and drain regions.

29. The thin film transistor of claim 25 wherein the thin film transistor is provided relative to a supporting substrate, the channel annulus being longitudinally elongated and oriented substantially perpendicularly relative to the substrate.

30. A thin film transistor comprising:

a thin film transistor layer having a source region, a channel region and a drain region; the thin film channel region comprising an annulus; and

a gate in proximity to the thin film channel annulus, the gate comprising an annulus which surrounds the thin film channel annulus.

31. The thin film transistor of claim 30 wherein the channel annulus and the gate annulus are longitudinally elongated.

32. The thin film transistor of claim 30 wherein at least one of the source region or the drain region is elongated and the channel region is elongated, the channel region being oriented substantially perpendicularly relative to the one region.

33. The thin film transistor of claim 30 wherein the source region and the drain region are oriented parallel relative to one another, the channel region being oriented substantially perpendicularly relative to the source and drain regions.

34. The thin film transistor of claim 30 wherein the thin film transistor is provided relative to a supporting substrate, the channel annulus and the gate annulus being longitudinally elongated and oriented substantially perpendicularly relative to the substrate.

35. A thin film transistor comprising:

a base layer having a locally substantially planar outer surface;

a thin film transistor layer provided outwardly of the base layer outer surface; the thin film layer having a source region, a channel region and a drain region; at least one of the thin film source region or the thin film drain region being elongated and oriented substantially parallel with the base layer outer surface; the thin film channel region consisting essentially of a region elongated in a direction substantially perpendicular to the base layer outer surface; and

a gate in proximity to the thin film channel region, the gate being elongated in a direction substantially perpendicular to the base layer outer surface along the thin film channel region.

Add A27

Add B27

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